SEMICONDUCTOR DEVICE HAVING A FERROELECTRIC TFT AND A DUMMY ELEMENT

FIELD OF THE INVENTION

The present invention relates to a semiconductor device. More particularly the present invention relates to a semiconductor device including a semiconductor element such as a capacitor and a transistor in which a dielectric with high dielectric constant or a ferroelectric is used.

BACKGROUND OF THE INVENTION

With increases in the packing density of semiconductor memories, a capacitor element with larger capacity is needed. Therefore, a technology to integrate a capacitor element including a dielectric layer with high dielectric constant or a ferroelectric characteristics into a integrated circuit lately has attracted considerable attention.

In order to put a nonvolatile RAM into practice which enables writing and reading with lower operating voltage at higher speed compared to conventional devices, a technology to integrate a capacitor element including a ferroelectric layer has been pursued.

A conventional method for manufacturing a semiconductor device including a dielectric with high dielectric constant or a ferroelectric characteristics (hereinafter, a dielectric with high dielectric) is explained below referring to FIGS. **20**A and **20**B.

As shown in FIG. **20**A, a first metal film **202** (e.g. a Pt film) is formed on a substrate **201** with an integrated circuit by sputtering. A dielectric film **203** with high dielectric constant is formed on the first metal film **202** by spin coating or chemical vapor deposition (CVD), followed by forming a second metal film **204** (e.g. a Pt film) on the dielectric film **203** by sputtering. After a photoresist **209** is formed on the second metal film **204** in a predetermined pattern, each film is selectively removed by dry etching to form a capacitor element **208** composed of first electrode **205**, a capacitor dielectric layer **206** and a second electrode **207**.

However, in such a capacitor element produced by the conventional method, a capacitor dielectric layer with high dielectric constant is degraded in electric characteristics. Such a degradation also is observed in a transistor including a dielectric layer with high dielectric constant.

SUMMARY OF THE INVENTION

Therefore, with the foregoing in mind, it is the object of the present invention to suppress a degradation of a dielectric with high dielectric constant in a semiconductor element.

In order to achieve the above-described object, an embodiment of the semiconductor device of the present invention comprises a substrate, a semiconductor element and a dummy semiconductor element. The semiconductor element includes a first dielectric layer on the substrate and an electrode on the first dielectric layer, and the dummy semiconductor element includes a second dielectric layer on the substrate and a dummy electrode on the second dielectric layer. The dummy semiconductor is located so that a space between the electrode and the dummy electrode is in a predetermined range. The predetermined range is preferably between 0.3 μm and 1.4 μm.

When the semiconductor element is a capacitor element, an embodiment of the semiconductor device of the present invention comprises a substrate, a capacitor element and a dummy capacitor element. The capacitor element includes a bottom electrode on the substrate, a first dielectric layer on the bottom electrode and a top electrode on the first dielectric layer, and the dummy capacitor element includes a dummy bottom electrode on the substrate and a second dielectric layer on the dummy bottom electrode and a dummy top electrode on the second dielectric layer. The dummy capacitor element is located so that a space between the top electrode and the dummy top electrode is in a predetermined range (e.g. 0.3 μm to 14 μm).

Two or more semiconductor elements can be included in the semiconductor device. In such a case, an embodiment of the semiconductor device of the present invention comprises a substrate, at least two capacitor elements, and a dummy capacitor element. Each capacitor element includes a bottom electrode, a first dielectric layer and a top electrode, and the dummy capacitor element includes a dummy bottom electrode, a second dielectric layer and a dummy top electrode as described above. The capacitor elements and the dummy capacitor element are located so that a space between an adjacent pair of electrodes selected from the top electrodes and the dummy top electrode, in which at least one electrode in the pair is one of the top electrodes, is in a predetermined range (e.g. 0.3 μm to 14 μm). The semiconductor device can include two or more dummy semiconductor devices.

Such a semiconductor device of the present invention can be manufactured by a method which comprises forming a dielectric film on a substrate, forming the electrically conductive film on the dielectric film, and etching the electrically conductive film so as to form the electrode. When etching the electrically conductive film, a dummy electrode is formed with the electrode so that a space between the electrode and the dummy electrode is in a predetermined range (e.g. 0.3 μm to 14 μm).

The inventors have succeeded in elucidating the degradation of the dielectric with high dielectric constant in a semiconductor element.

As shown in FIGS. **20**A and **20**B, the second metal film **204** is etched until the surface of the dielectric film **202** appears. As shown in FIG. **21**, in the dry etching, etching ions **210** are partially accumulated on the dielectric film **203** so that the surface of the dielectric film **203** holds electrical charges **211**. In the case of a dielectric with high dielectric constant, the amount of electrical charges **211** is around 100 times as much as that in the case of silicon oxide or silicon nitride. The amount of electrical charges is proportional to the area of the surface exposed to the etching ions **210**.

Therefore, the large exposed surface of the dielectric film **203** with high dielectric constant causes an electrostatic repulsion between the etching ions **210** and the electrical charges **211**. As shown in FIG. **21**, the repulsion changes the direction of travel **212** of the etching ions **210** around the photoresist **209**. The etching ions **210** deviate to the dielectric covered with the metal layer **207**, which will remain as a dielectric layer of a capacitor element. More collision of etching ions **210** with the dielectric below the edge portion of the metal layer **207** than usual generates defects in the crystal structure in the dielectric. Thus, a damaged region **213**, which causes the degradation in the capacitor element, is formed.

According to the present invention, the surface of the dielectric film exposed to the etching ions is limited by the dummy element, which can reduce the electrical charges on the dielectric film. Therefore, the collision with the etching ions proceeding diagonally is suppressed to prevent the semiconductor element from degrading in electrical characteristics.